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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/444,819	11/22/1999	SHUICHI KIKUCHI	10417-006001	9133

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FISH & RICHARDSON P.C.  
45 ROCKEFELLER PLAZA, SUITE 2800  
NEW YORK, NY 10111

EXAMINER

RAO, SHRINIVAS H

ART UNIT PAPER NUMBER

2814

DATE MAILED: 12/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/444,819

Applicant(s)

KIKUCHI ET AL.

Examiner

Steven H. Rao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 September 2002.
- 2a) ☐ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4,8-10,17 and 19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-4,8-10,17 and 19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All   b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

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### DETAILED ACTION

Applicants' appeal brief filed on September 19, 2002 has been entered on September 25, 2002.

Therefore claims 1-4, 8-10, 17 and 19 as recited in applicants' appeal brief are currently pending in the application.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-2, 8 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwon et al. ( U.S. Patent No. 5,907,173 herein after Kwon)

With respect to claim 1 Kwon describes a semiconductor device including : a source region ( Kwon fig. 4 # 45, col. 5 line 41), a channel region ( Kwon fig.4 # area below gate 44), a drain region ( fig.4 # 47, col. 5 line 43), a gate electrode disposed

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above the channel region ( fig. 4 #44, col. 5 line 44), and a drift region disposed adjacent to the channel region and extending to and below the drain region ( Fig.4 # 43), and wherein the drift region is formed shallowly at least below the gate electrode but formed deeply in a neighborhood of the drain region. ( fig. 4 # 43).

With respect to claim 2, Kwon describes a semiconductor device including :

A first conductivity type well region formed in a first conductivity type semiconductor substrate ( Kwon fig. 1 p-well ), a gate electrode formed on the substrate via a gate insulating film (Fig.1 # 4-a gate electrode and # 32 gate insulating film), a first conductivity type body region ( fig. 1 # 6) formed adjacent to the gate electrode , a second conductivity type source region ( fig. 1 # 5) and a channel region formed in the first conductivity body region ( fig.1 region below gate 4), a second conductivity type drain region formed at a position remote from the first conductivity type body region. ( fig.1 # 7) and a second conductivity type drift region formed shallowly from the channel region to the drain region, at least below the gate electrode and formed deeply in a neighborhood of the drain region. ( Kwon fig.1).

With respect to claim 8, wherein a semiconductor device comprising a first Mos ( Kwon col. 1 line 19) transistor having a source region ( Kwon fig. 4 # 45, col. 5 line 41), a channel region ( Kwon fig.4 # area below gate 44), a drain region ( fig.4 # 47, col. 5 line 43), a gate electrode formed on the channel region ( fig. 4 # 44, col. 5 line 44), and a drift region formed between the channel region and the drain region ( Fig.4 # 43), and a second Mos transistor having a source region, a channel region, a drain region and a gate region formed on the channel region . (Kwon col.4 line 53 ) ; and wherein the drift

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region of the first Mos transistor is formed shallowly at least below the gate electrode but formed deeply in a neighborhood of the drain region. (Kwon fig. 4 ) ; and a source / drain region of the second MOS transistor consists of a low concentration source/drain region ( Kwon fig. 3 and col. 4 lines 63), a high concentration source-drain region ( Kwon col.5 line 4-5) and a middle concentration source/drain region whose concentration is higher than that of the low concentration source/drain region but lower than that of the high concentration source/drain region. (Kwon figs. 5 E to G).

With respect to claim 19, wherein the second conductive type drift region is formed to be adjacent to the first conductive type body region. ( Kwon figs. 1,4 etc.).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-4, 9-10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. ( U.S. Patent No. 5,907,173 herein after Kwon) as applied to claims 1-2 and 19 above and further and in view of Blanchard et al. ( U.S. Patent No. 5,869,371 herein after Blanchard) .

With respect to claim 3, Kwon describes a semiconductor device including :  
a second conductivity type drift region . The limitation," wherein the second conductivity type drift region is formed by implanting at least two kind second

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conductivity type impurities which have different diffusion coefficients and at least one kind first conductivity type impurity which has a diffusion coefficient substantially equal to or larger than the diffusion coefficient of at least one kind second conductivity type impurity such that it is formed by diffusing the second conductivity type impurities in to a deep region by using a difference in the diffusion coefficients and is formed shallowly in a neighborhood of the source region by canceling the second conductivity type impurities by the first conductivity type impurity " in claim 3 is taken to be product-by – process limitations and non limiting. A product-by –process claim is directed to the product per se, no matter how actually made. See *In re Fessman* 180, USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 ( Fed. Cir. 1983) and *In re Thrope* 227 USPQ 964, 966 (Fed. Cir. 1985).

With respect to claim 4, wherein the second conductivity type drift region is formed by implanting an arsenic ion and a phosphorous ion as the second conductivity type impurities in to an overall surface region serving as the drift region and selectively implanting a boron ion as the first conductivity type impurity only into a region in a neighborhood of the source region.

The limitation," the second conductivity type drift region is formed by implanting an arsenic ion and a phosphorous ion as the second conductivity type impurities in to an overall surface region serving as the drift region and selectively implanting a boron ion as the first conductivity type impurity only into a region in a neighborhood of the source region. " in claim 4 is taken to be product-by –process limitations and non limiting. A product-by –process claim is directed to the product per se, no matter how actually

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made. See *In re Fessman* 180, USPQ 324, 326 ( CCPA 1974); *In re Marosi et al.* , 218 USPQ 289, 292 ( Fed. Cir. 1983) and *In re Thrope* 227 USPQ 964, 966 (Fed. Cir. 1985).

With respect to claim 9, wherein the a semiconductor device comprising a first Mos ( Kwon col. 1 line 19) transistor and a second Mos transistor (Kwon col.4 line 53 ) formed on the first conductivity type substrate (Kwon fig. 4) wherein the first Mos transistor includes a first conductivity type well region formed in the semiconductor substrate ( Kwon fig. 1 p-well ), a first gate electrode formed on the first conductivity type well region via a first gate insulating film (Fig.1 # 4-a gate electrode and # 32 gate insulating film), a first conductivity type body region ( fig. 1 # 6) formed adjacent to the gate electrode , a second conductivity type source region ( fig. 1 # 5) and a channel region formed in the first conductivity body region ( fig.1 region below gate 4), and a second conductivity type drain region ( Kwon fig. 1 # 7) region formed at a position remote from the first conductivity type body region (Kwon fig.1 # 7) a second conductivity type drift region formed shallowly from the channel region to the drain region, at least below the gate electrode and formed deeply in a neighborhood of the drain region. ( Kwon fig.1).

Wherein the second Mos includes : a second conductivity type well region formed in the semiconductor substrate .

Kwon does not specifically mention a second conductivity type well.

However, Blanchard a patent from the same filed of endeavor, describes in fig.5 B etc. a second conductivity type well to provide deep body depths and spacing in

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relation to the epitaxial layer's depth and doping so that depletion boundaries from the body potential will pinch off the channel of the parasitic JFET and thereby protect the channel from high voltages.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Blanchard's second conductivity type well in Kwon's method to provide deep body depths and spacing in relation to the epitaxial layer's depth and doping so that depletion boundaries from the body potential will pinch off the channel of the parasitic JFET and thereby protect the channel from high voltages. (Blanchard col. 9 lines 40-50).

The other limitations of claim 9 are : a second gate electrode formed on second conductivity type well region via a second gate insulating film (Blanchard fig. 2 F), and a source / drain region consisting of a low concentration source/drain region formed adjacent to the second gate electrode ( Kwon fig. 3 and col. 4 lines 63), a high concentration source-drain region ( Kwon col.5 line 4-5) and a middle concentration source/drain region whose concentration is higher than that of the low concentration source/drain region but lower than that of the high concentration source/drain region. (Kwon figs. 5 E to G).

With respect to claim 10, wherein the first Mos transistor consists of an N-Channel LDMOS transistor and the second Mos transistor consists of a P- Channel high breakdown voltage Mos transistor ( Kwon col. 4 lines 58- col. 5 lines 45).

With respect to claim 17, wherein the semiconductor device is arranged in plural via a element isolation film and a channel stopper layer is formed under the element

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isolation film. (Blanchard fig. 2g # 134, col. 6 line 14 and fig., 2G # 130, col. 6 line 14-15).

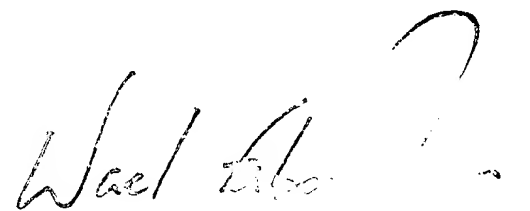
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.



Steven H. Rao  
Patent Examiner  
December 3, 2002



SUPERVISORY PRINCIPAL EXAMINER  
TECHNOLOGY CENTER 2000